AMENDEMENTS TO THE SPECIFICATION

Please replace paragraph [0038] of the Specification with the following amended paragraph:

[0038] When user data is read from a sector of an erase block of the Flash memory 200, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. For example, User Data A read from the user data area 220 of Sector 0 218 of Erase Block 0 216 will have its Overhead Data (Ovhd A) read from the overhead data area 232 of Sector 0 234 of Erase Block 1 226; User Data B read from the user data area 230 of Sector 0 [[228]] 234 of Erase Block 1 226 will have its Overhead Data (Ovhd B) read from the overhead data area 222 of Sector 0 218 of Erase Block 0 216.

Please replace paragraph [0045] of the Specification with the following amended paragraph:

[0045] In moving, the source physical row page 310, containing the data sectors 302 and overhead/ECC data areas 304 to be moved 314, is read from the source erase block of the Flash memory device into the internal data latches (not shown). Selected data sectors 302 and overhead/ECC data areas 304 are read from the memory device from the internal latches. Typically the selected data sectors 302 and overhead/ECC data areas 304 are read from the memory device to be externally checked for ECC errors. Any sector data 302 and overhead/ECC data areas of the source physical row page [[350]] 310 that are not to be moved to the target physical row page 312 of the target erase block (which may be the same erase block as the source erase block) is masked off. This is typically done in Flash memory by writing "FF" data (logical 1's) to the portion of the internal data latches that contain the undesired data sectors (Flash memory floating gate cells are in an erased state at logical "1" and program to logical "0", thus writing a logical "1" to a Flash memory cell maintains its current state). The modified contents of the internal data latches containing the logical data sectors 302 and overhead/ECC data areas 304 to be moved 314 are then written to the target physical row page 312.

Please replace paragraph [0046] of the Specification with the following amended paragraph:

[0046] Figure 3B details a split data move operation with a corresponding sequential pair of data split Flash memory physical row pages 350, 352 of a NAND architecture Flash memory device array of an embodiment of the present invention. During the move a selected set of logical sectors 358 and associated overhead data/ECC areas 360 are moved from the source pair of data split Flash memory physical row pages 350, 352 to a target sequential pair of data split Flash memory physical row pages 354, 356. Each physical page of pair of physical pages (source pair 350, 352 and target pair 354, 356) are paired across two erase blocks for fault tolerance purposes (Erase Block A and Erase Block B). The physical pages 350, 352, 354, 356 of Figure 3B each contain 2112 bytes of data and are formatted to contain four 512-byte logical sectors 302. In addition, space is provided at the beginning of the physical ~~page 300~~ pages 350, 352 for four overhead data areas/ECC codes 304 of 8 bytes each. A further 32 bytes 306 is reserved for use by the EBM firmware or other system level usage.

Please replace paragraph [0064] of the Specification with the following amended paragraph:

[0064] Due to the formatting structure of the split data physical row page 350, 352 and the non-split data physical row page [[301]] 310, the ECC/overhead data and the sector data are typically contiguous. In the split data physical row page 350, 352, with the ECC data 304 coming before the sector data 302, the final ECC codes of the current physical row page (associated with the sectors of the previous physical row page) abut the initial data sectors of the current physical row page. In the non-split data physical row page 310, the associated ECC data 304 trailing the selected sector data 302. As a result of this, only a contiguous range of column addresses need be moved from any split or non-split data source physical row page. In addition, while masking can occur in data move operations that span multiple contiguous source physical rows, the data move operation may also simply move any contiguous intermediate physical row pages as whole rows and not mask any data, although masking may also occur, loading the A and B Pre-Count Counters 422, 428, Post Address Registers 424, 430, and Post-Count Counters 426, 432 with zeros. In this, the external address generation hardware in split data embodiments operates the A/B select lines 436 to toggle selection of the current A/B target and source physical

page rows, the row increment signal line 438 to increment to the next sequential row addresses, and Zero Row signal lines 440 to wrap around in the A/B source and target erase blocks during movement of data from more that two physical row pages. Because they may only select a portion of a physical page row, the final two physical row pages of a split data multiple contiguous source physical row data move operation (and the single final row of a non-split data multiple contiguous source physical row data move operation) utilize a data mask, as the two initial physical row pages can, to select only the data (sector 302 and ECC codes 304) that is to be moved. As the number of data sectors moved decrease, the initial two physical row page move operations and final row data move operations will merge until, when the data sectors to be moved reside on only the initial source A physical row page, only a single pair of data split physical row pages are accessed (in this case the move operation only needs to move the data sectors from source A physical row page and the associated ECC codes from source B physical row page). It is noted that the moves of intermediate source physical row pages, since they move an entire physical row page, can also be accomplished with a conventional copy-back command operation.

Please replace paragraph [0066] of the Specification with the following amended paragraph:

[0066] After the read operation is executed the split data move control circuit 400 requests status by placing a "70" status request 518 on the data bus and latching it into the NAND architecture Flash memory device execution logic via a pulse on the CLE signal line 522. The data clock on the WE# line is then stopped and the read enable (RE#) is asserted active low 530 to reverse the direction of the data bus. The NAND architecture Flash memory device then asserts a "busy" (status code "80") 526 on the data bus until the selected physical row page has been retrieved from the memory array and is present in the internal data latches, at which point the asserted status code on the data bus changes to "ready" (status code "E0") 528. In addition, at this time the NAND architecture Flash memory device releases the R/B# line [[530]] 544 and allows it to go inactive. It will be appreciated by those skilled in the art that the R/B# line in some embodiments may be utilized to exclusively track the status of the NAND architecture Flash memory device. However, as NAND architecture Flash memory systems can comprise one or more memory devices and the R/B# line is common amongst the devices and can be

overdriven by another memory device in the system, it may not always be an indicator of the status of the device being operated on. As a result, in these situations directly requesting status of the memory device being operated on via the data bus is a more direct measure of device status.